IN THE CLAIMS

Claims 1 – 9 and 11 – 30 have been cancelled. Claims 31 – 58 have been added.

Claims 1 – 30 (cancelled).

31. (new) A system to manage energy usage of a processor, comprising:

a data communication network;

a transmitter, coupled to the data communication network, to invoke a protocol state machine to send a packet and to wait for an acknowledgment of receipt;

a receiver, in communication with the transmitter coupled to the data communication network, to receive, process, and verify the packet and to send the acknowledgment of receipt of the packet;

a buffer, coupled to the protocol state machine in the transmitter, to store an incoming packet to be transmitted by the transmitter; and

a processor, coupled to the protocol state machine in the transmitter,

wherein the protocol state machine manages a power level of the processor based on a utilized capacity of the buffer.

32. (new) The system of claim 31, wherein the data communication network includes at least one of the Internet and an Intranet.

33. (new) The system of claim 31, wherein the processor in the transmitter begins in a high power, high clock rate mode.

34. (new) The system of claim 31, wherein the transmitter performs tasks to create packets for transmission, the tasks including at least one of dividing data into packets, adding protocol headers, or computing checksums.

35. (new) The system of claim 31, wherein the processor enters a low power, low clock rate mode while waiting for the acknowledgment of receipt of the packet from the receiver.

36. (new) The system of claim 35, wherein the transmitter awakens when the incoming packet buffer reaches a low water mark.

37. (new) The system of claim 31, wherein the receiver includes an application buffer and after the receiver receives the packet, the packet is stored in the application buffer.

38. (new) The system of claim 37, wherein the receiver includes a receiver protocol state machine and a receiver processor, and the receiver protocol state machine manages a power level of the receiver processor based on a utilized capacity of the application buffer.

39. (new) The system of claim 37, wherein the receiver processor begins in a low power, low clock rate mode.

40. (new) The system of claim 37, wherein the receiver processor enters a high power, high clock rate mode when the application buffer reaches a maximum capacity.

41. (new) An article comprising:

a computer-readable storage medium having stored thereon instructions that when executed by a computer result in the following:

receiving a data packet at a receiver protocol state machine, the data packet being transmitted from a transmitter protocol state machine over a data communication network;

depositing the data packet in an application buffer;

processing and verifying the data packet; and

transmitting an acknowledgment of receipt of the data packet to the transmitter protocol state machine, wherein the receiver protocol state machine manages a power level of a processor coupled to the receiver protocol state machine based on a utilized capacity of the application buffer.

42. (new) The article of claim 41, including instructions, which when executed by the computer result in the processor entering a high power, high clock rate mode when the application buffer reaches a maximum capacity.

43. (new) The article of claim 42, including instructions, which when executed by the computer result in the processor entering an idle low power, low clock rate mode after the application buffer has reached the maximum capacity and the receiver protocol state machine has processed packets residing in the application buffer.

44. (new) The article of claim 41, wherein the utilized capacity of the application buffer and a timer cause periodic patterns in data packet reception, which are used to manage power and frequency of a processor in a transmitting device.

45. (new) The article of claim 41, wherein the data communication network includes at least one of the Internet and an Intranet.

46. (new) A receiver for managing energy usage of a processor, comprising:

a protocol state machine to receive a packet from a transmitter over a data communication network and to process and verify the packet;

a processor coupled to the protocol state machine; and

an application buffer coupled to the protocol state machine to store the packet,

wherein the protocol state machine transmits an acknowledgment of receipt of the data packet to the transmitter and the protocol state machine manages a power level of the processor based on a utilized capacity of the application buffer.

47. (new) The receiver of claim 46, wherein the processor enters a high power, high clock rate mode when the application buffer reaches a maximum capacity.

48. (new) The receiver of claim 46, wherein the processor enters an idle low power, low clock rate mode after the application buffer has reached the maximum capacity and the receiver protocol state machine has processed packets residing in the application buffer.

49. (new) The receiver of claim 46, wherein the application buffer and a timer cause periodic patterns in data packet reception, which are used to manage power and frequency of a processor in a transmitting device.

50. (new) A method of managing energy usage of a processor, comprising:

receiving a data packet at a receiver protocol state machine, the data packet being transmitted from a transmitter protocol state machine over a data communication network;

depositing the data packet in an application buffer;

processing and verifying the data packet; and

transmitting an acknowledgment of receipt of the data packet to the transmitter protocol state machine, wherein the reciever protocol state machine manages the a power level of the processor, coupled to the receiver protocol state machine, based on a utilized capacity of the application buffer.

51. (new) The method of claim 50, the processor entering a high power, high clock rate mode when the application buffer reaches a maximum capacity.

52. (new) The method of claim 51, the processor entering an idle low power, low clock rate mode after the application buffer has reached the maximum capacity and the receiver protocol state machine has processed packets residing in the application buffer.

53. (new) The method of claim 51, wherein the application buffer and a timer cause periodic patterns in data packet reception, which are used to manage power and frequency of a processor in a transmitting device.

54. (new) The method of claim 51, wherein the data communication network includes at least one of the Internet and an Intranet.

55. (new) A method of managing energy usage of a processor in a transmitting device, comprising:

invoking a protocol state machine to send a packet across a data communication network to a receiver and waiting for an acknowledgment of receipt;

storing incoming packets that are to transmitted by the protocol state machine to the receiver in a buffer; and

managing a power level of the processor in the transmitting device based on a utilized capacity of the buffer.

56. (new) The method of claim 55, wherein after the packet has been transmitted, the protocol state machine switches the power level of the processor to a low power, low rate clock mode.

57. (new) The method of claim 56, wherein when the utilized capacity of the buffer reaches a threshold value, the protocol state machine switches the power level of the processor to a high power, high rate clock mode.

58. (new) The method of claim 57, wherein the protocol state machine does not transmit any of the packets in the buffer until the utilized capacity of the buffer reaches the threshold.